Industry-Leading Transistor Performance Demonstrated on Intel's 90-nanometer Logic Process

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What are We Announcing?

Industry-leading transistor performance has been demonstrated on Intel's 90 nm process technology using these unique process features:

- **1.2 nm gate oxide** — Thinnest in the industry
- **Strained silicon** — First to commit this performance enhancing technique to production

The integrated 90 nm process is demonstrating high yield on a 52 Mbit SRAM memory chip

- **1.2 nm oxide + strained silicon transistors**
- **7 copper layers + new low-k dielectric**
- **1.0 μm^2 SRAM memory cell size**
- **300 mm wafers**

Why is this Important?

- Shows that Intel is well on track, delivering a new process technology every 2 years
- Each new generation allows higher clock rates and more transistors at lower cost, delivering more value to the end user
- This development will enable products with higher performance that use less power
- Demonstrates that Intel technology evolution continues to follow Moore's Law

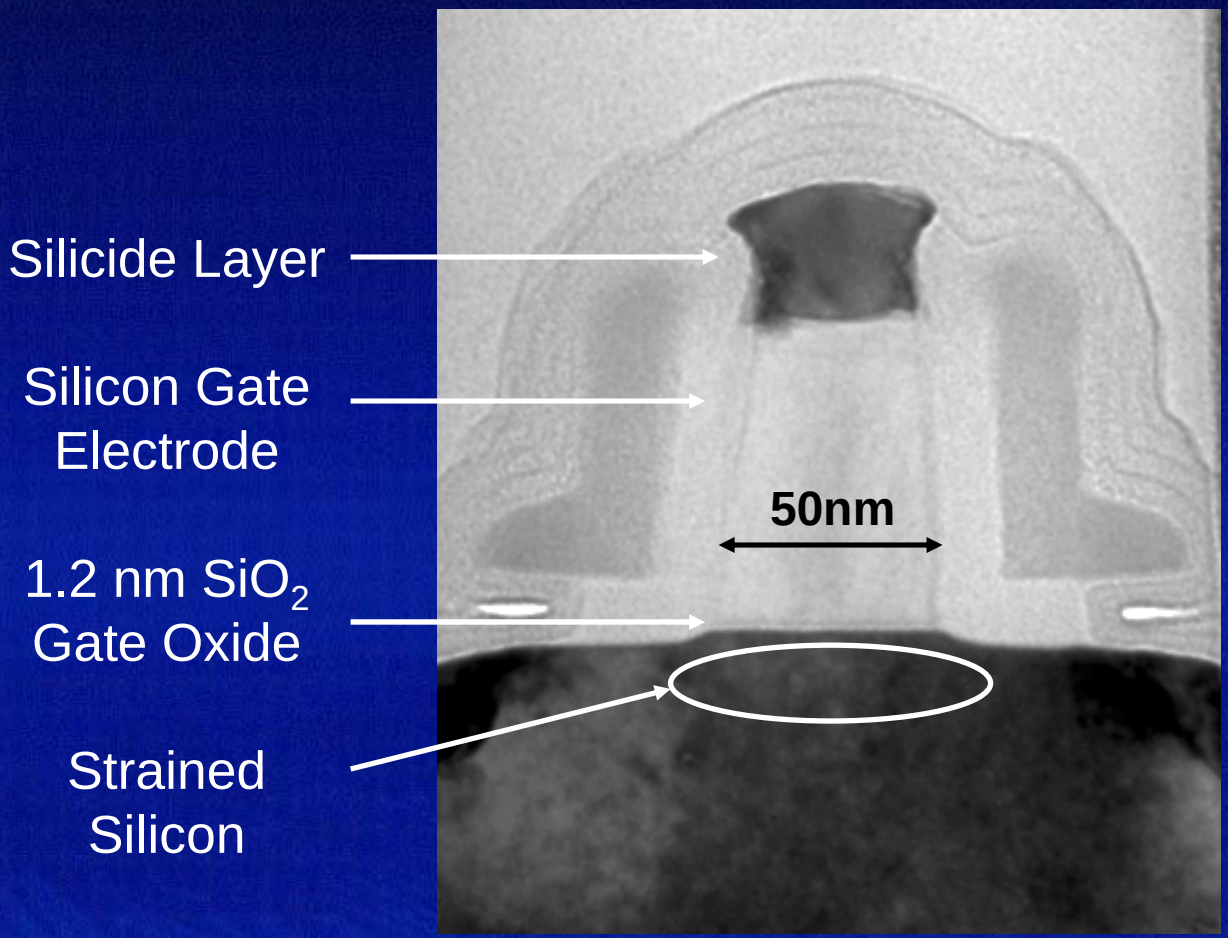
A New Process Every 2 Years

Process Name	P854	P856	P858	Px60	P1262	P1264
1st Production	1995	1997	1999	2001	2003	2005
Lithography	0.35µm	0.25µm	0.18µm	0.13µm	90nm	65nm
Gate Length	0.35µm	0.20µm	0.13µm	<70nm	<50nm	<35nm
Wafer (mm)	200	200	200	200/300	300	300

Moore's Law continues!

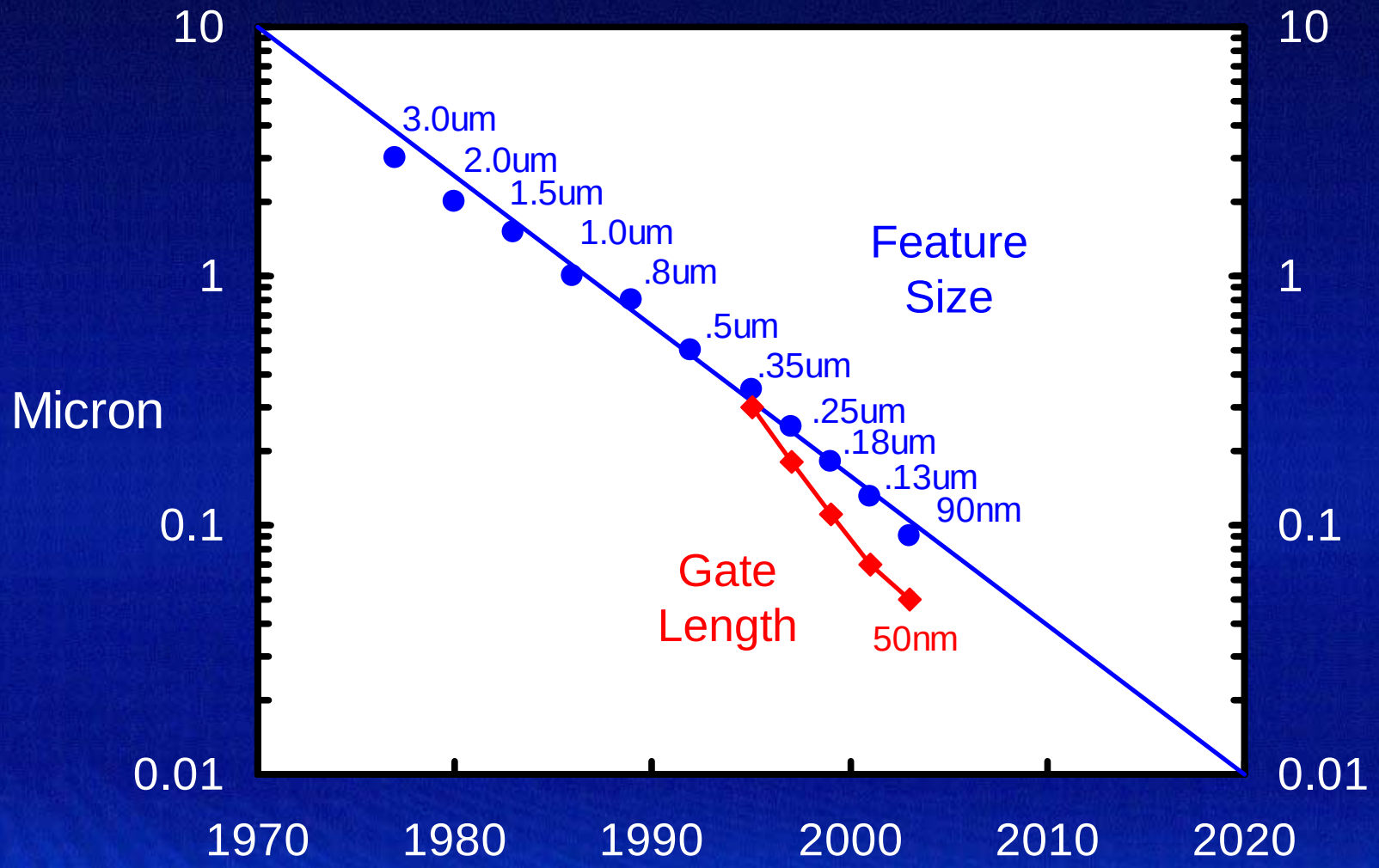
- *Intel has been introducing new technology generations on a faster 2 year interval since 1989*
- *We have technologies in Intel's R&D laboratories that will drive this pace of innovation into the next decade*

90 nm Generation Transistor



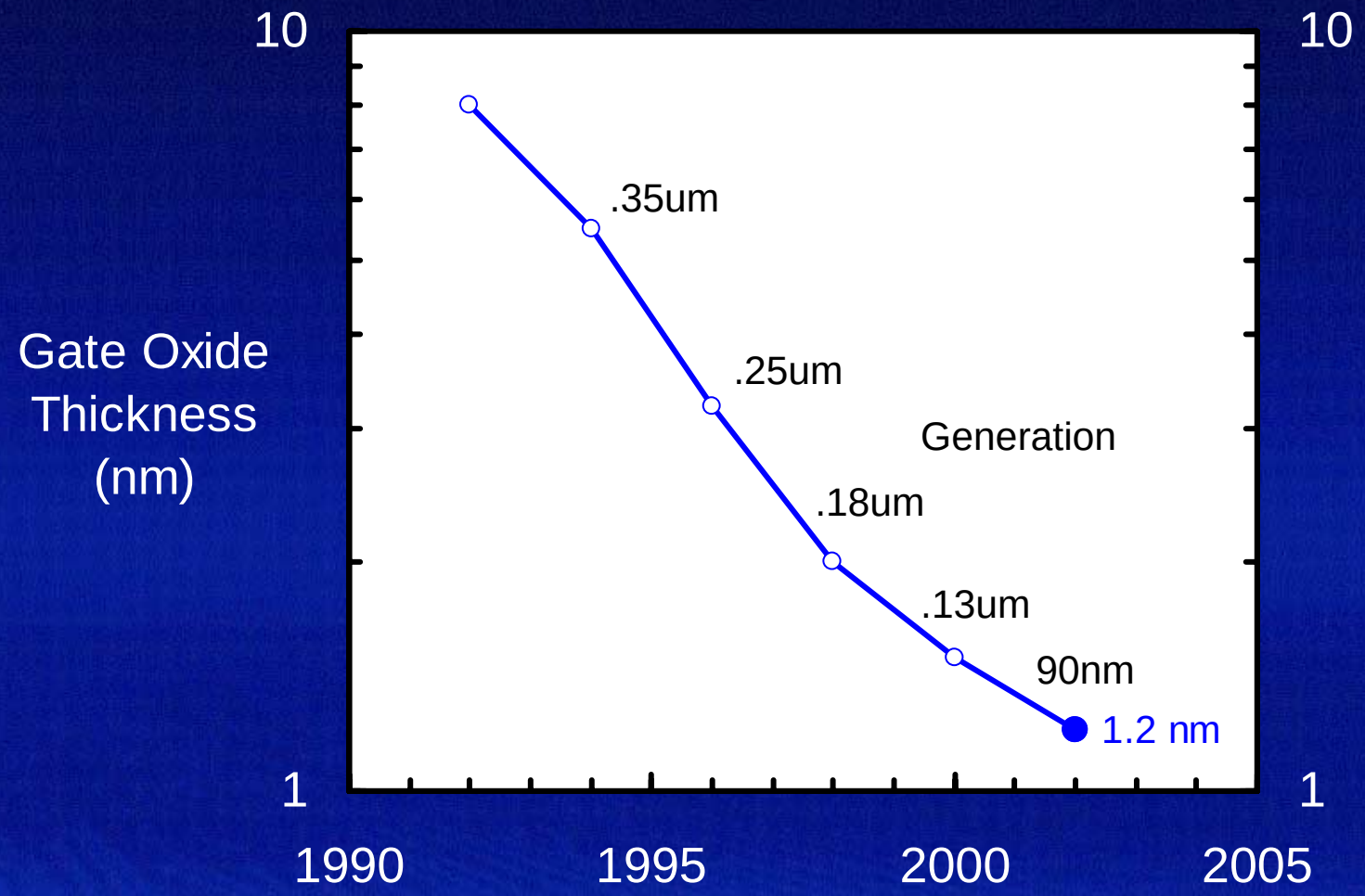
50 nm transistor dimension is ~2000x smaller than diameter of human hair

Transistor Gate Length Scaling



Faster gate length scaling to maintain transistor performance lead

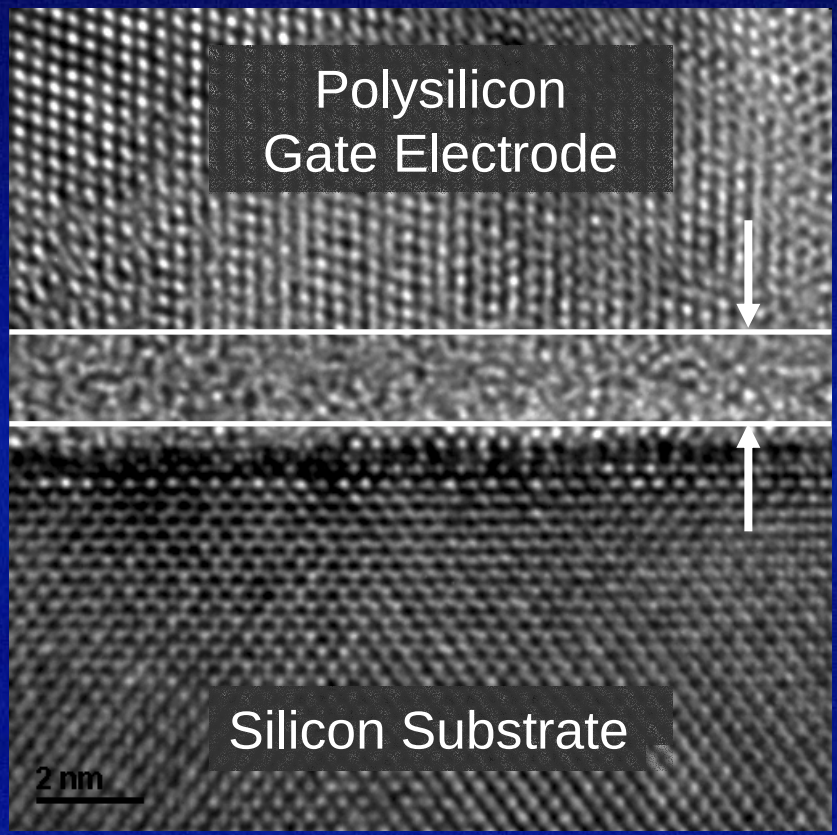
Gate Oxide Scaling



Intel leads the industry in gate oxide scaling

Thinner gate oxide increases transistor performance

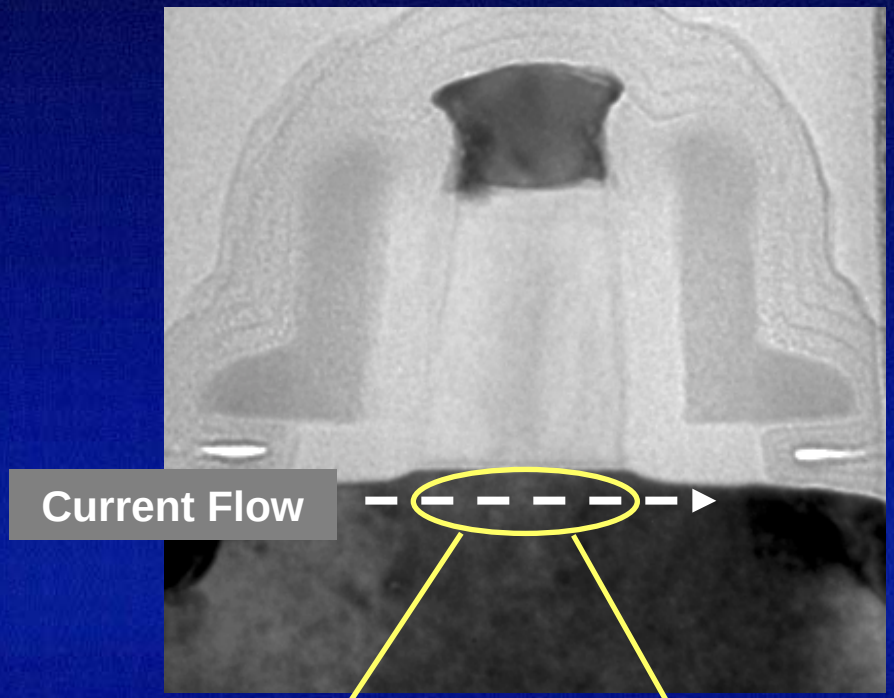
90 nm Generation Gate Oxide



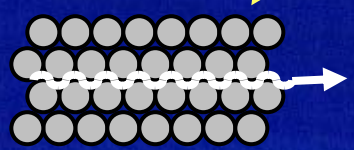
1.2 nm SiO_2

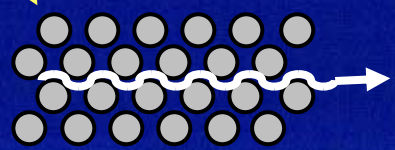
Gate oxide is less than 5 atomic layers thick

Strained Silicon Transistors



Normal electron flow





Faster electron flow

Normal Silicon Lattice

Strained Silicon Lattice

Strained Silicon Transistors

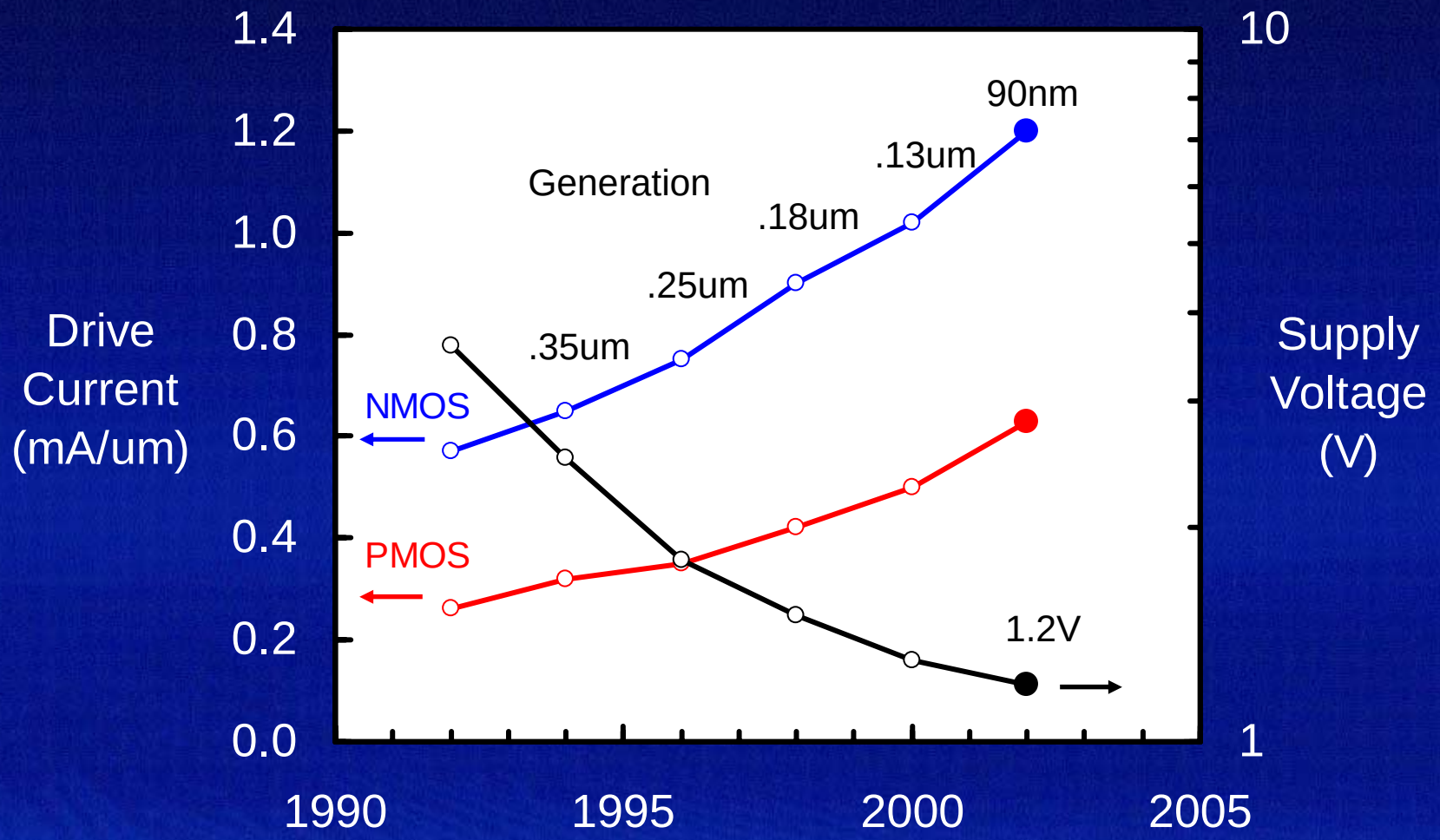
Strained silicon benefits

- Strained silicon lattice increases electron and hole mobility in transistor channels
- Greater mobility results in 10-20% increase in transistor current flow (drive current)
- Increased drive current = increased transistor performance
- Both NMOS and PMOS transistor performance improved

Strained silicon process

- Intel's strained silicon process is unique in the industry
- No detriments to transistor short channel behavior or junction leakage
- The added process steps increase total processing cost by only ~2%

Transistor Performance



Highest drive current in the industry

Reduced supply voltage for lower power

Transistor Summary

- 1.2 nm gate oxide thickness
  - Thinnest gate oxide in the industry, higher performance
- Strained silicon
  - Increases transistor drive current by 10-20 percent
- 50 nm gate length
  - Smaller dimension improves speed and reduces power
- Scaled supply voltage of 1.2V or less
  - Reduces chip power, especially important for mobile products
- Industry-leading transistor performance in a highly manufacturable process

A significant step towards the future TeraHertz transistor

90 nm Generation Interconnects

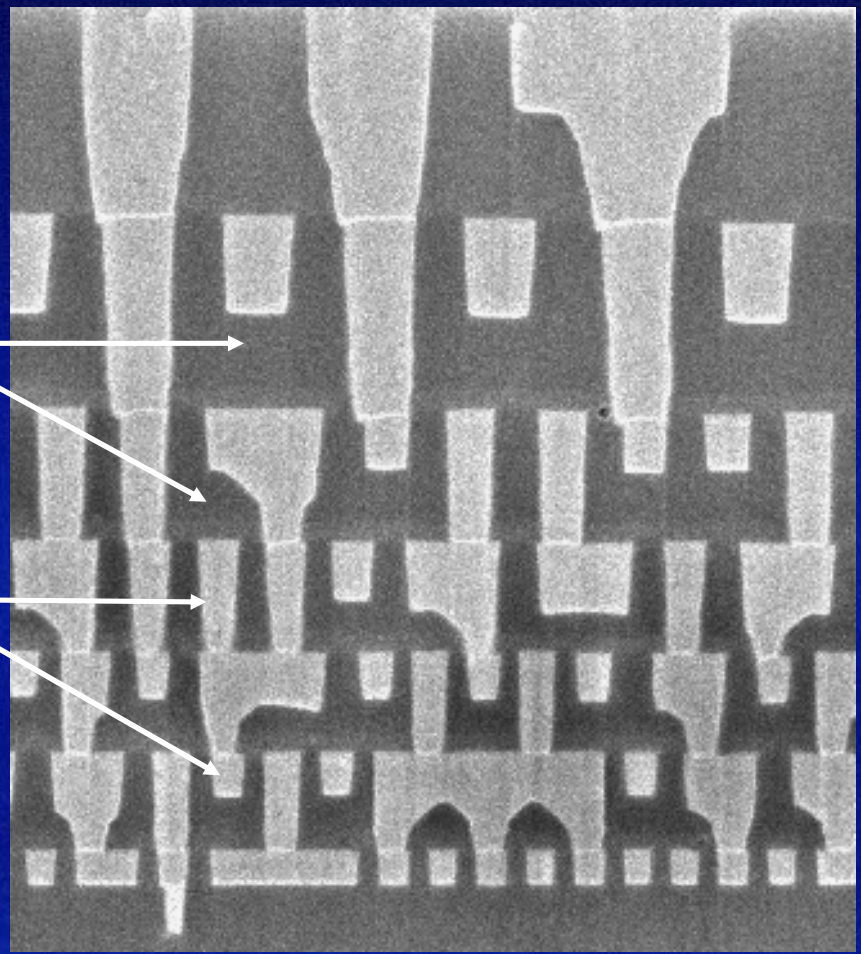
7 layers of copper interconnect

- 1 more layer than 0.13 μm generation
- Extra layer provides cost effective improvement in logic density

New low-k dielectric introduced to reduce wire-wire capacitance

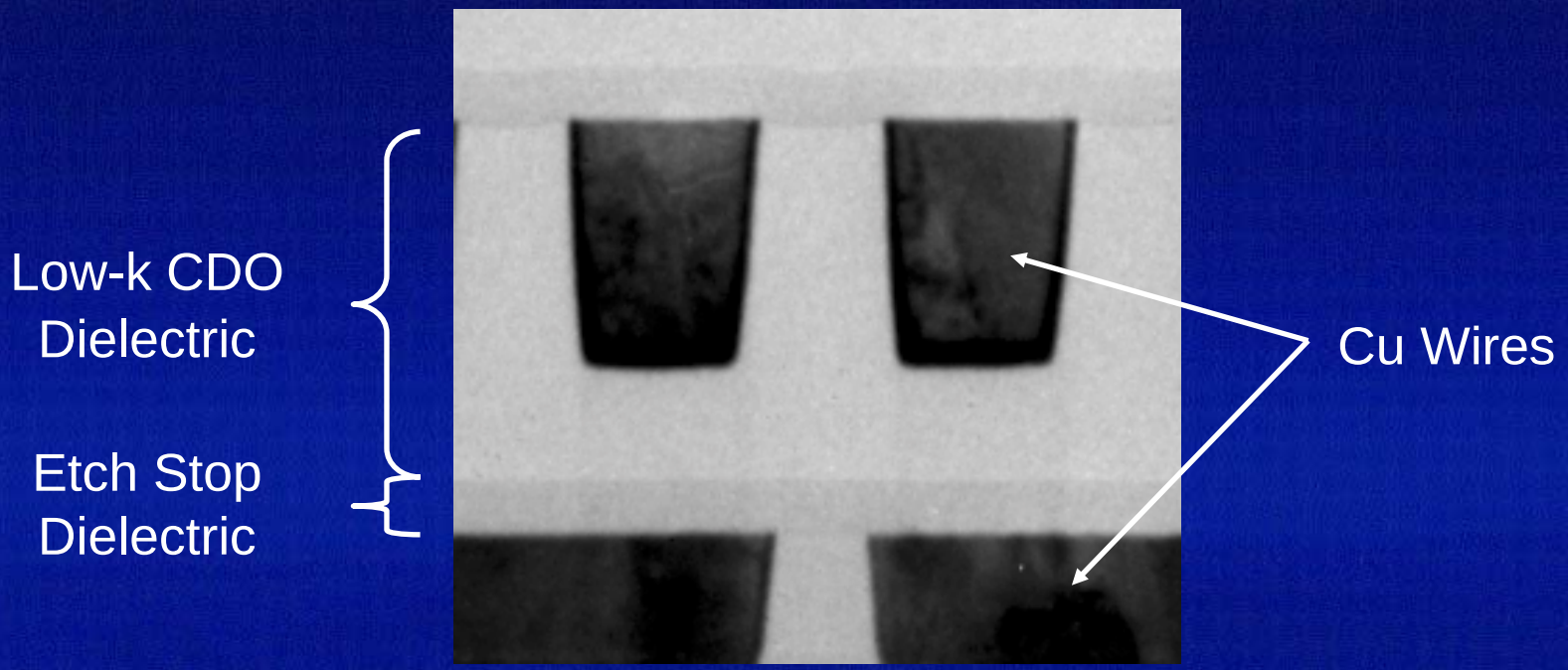
- Carbon-doped oxide (CDO) dielectric reduces capacitance by 18% compared to SiOF dielectric used on 0.13 μm
- Reduced capacitance speeds up intra-chip communication and reduces chip power
- Simple 2-layer dielectric stack used for low capacitance and low cost

90 nm Generation Interconnects



Combination of copper + low-k dielectric now meeting performance and manufacturing goals

Low-k CDO Dielectric



Simple 2-layer dielectric stack for low capacitance, low cost and ease of manufacturing

1.0 μm^2 SRAM Cell

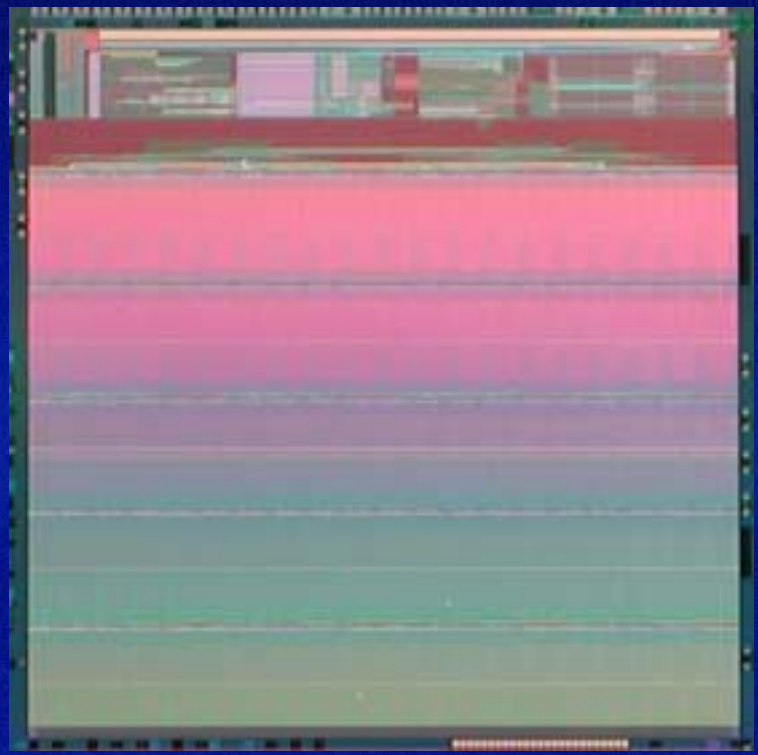
(as disclosed March '02)

- Ultra-small SRAM cell used in 90 nm process packs six transistors in an area of 1.0 μm^2
- Intel was first in the industry to reach this cell size milestone
- Small memory cell enables cost effective increase in CPU performance by adding more on-die cache memory

52 Mbit SRAM on 90 nm Process

(as disclosed March '02)

10.1 mm



10.8 mm

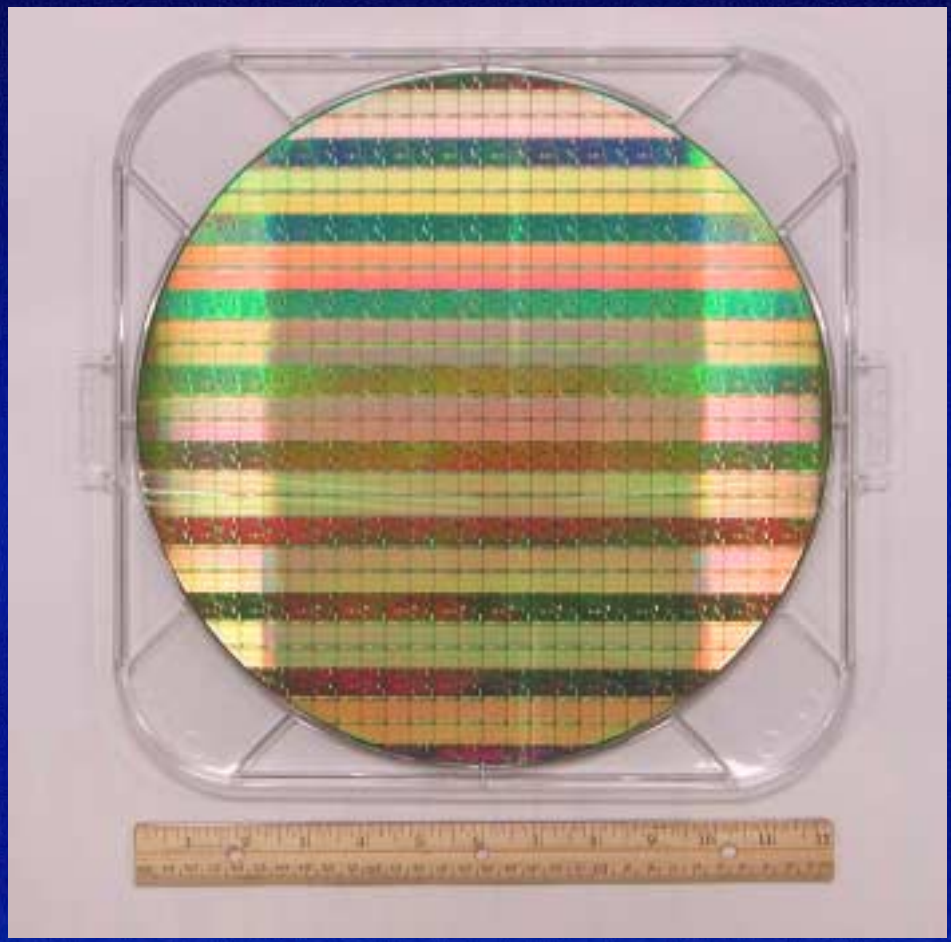
330 million transistors on single chip

Highest capacity SRAM in the industry

Perfect chips have been made with all 52 Mbits working

52 Mbit SRAM Chips on 300 mm Wafer

120 billion transistors on one wafer!



These 90 nm process wafers are being routinely produced in our Hillsboro, Oregon fab

Additional Manufacturing Details

- The 90 nm technology is being developed at Intel's 300 mm fab (D1C) in Hillsboro, OR
- 75% of process tools used on 300 mm version of 0.13 μm process are also used on the 90 nm process, lowering implementation costs
- A mixture of 248 nm and 193 nm wavelength lithography equipment is used
- The 90 nm process will be ramped to high volume in D1C and transferred to other 300 mm manufacturing fabs, starting in 2003
- The lead 90 nm product will be the processor codenamed *Prescott*, (next-generation processor based on NetBurst™ micro-architecture) to be introduced in second half of ’03

Summary

- Industry-leading transistor performance has been demonstrated using unique 1.2 nm gate oxide and strained silicon features
- High density, high performance interconnects are provided with 7 layers of copper combined with a new low-k CDO dielectric
- The manufacturability of this integrated technology has been demonstrated on 300 mm wafers with 52 Mbit SRAM chips using an ultra-small 1.0 μm^2 cell
- Intel has the world's most advanced 90 nm technology and will be first in volume manufacturing in 2003

Additional details of this 90 nm technology will be presented at the International Electron Devices Meeting (IEDM) in San Francisco in December 2002

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon